LOW NOISE BROADBAND MMIC AMPLIFIER CONCEPT

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ABSTRACT

Technique of the broadband, low-noise matching of the amplifier input by means of a lossless capacitive feedback is proposed. Bandwidth exceeding one decade with the noise figure on the order 1 - 1.5 dB and good input matching may be achieved with existing MMIC technologies, which is one of the best noise characteristics reported to date. Prototype 0.5 - 5 GHz amplifier achieves NF below 1.4 dB and good input matching.

INTRODUCTION

Well known techniques for broadbanding microwave amplifiers include: distributed and resistive feedback circuits (eg. [1]) which have no low-frequency limitations but are noisy, and balanced amplifiers which consume too much area to be feasible in the MMIC form below approx. 10 GHz. Series inductive feedback is successfully used in relatively narrowband amplifiers to obtain low noise and input matching. This paper proposes the application of the capacitive feedback, which may be used for bandwidths exceeding one decade with no degradation in noise properties. This technique requires accurate modeling and control of the circuit components to preserve amplifier stability and is feasible with the mature MMIC technology. The response of the amplifier is limited by the on-chip coupling capacitors and when these are attached externally, low frequency limit of the proposed technique may be extended below 100 MHz.

AMPLIFIER STRUCTURE

General structure of the amplifier is simple (Fig. 1) and consists basically of the low-noise main amplifier with high voltage gain and the phase and gain equalizer to provide the required feedback loop response.

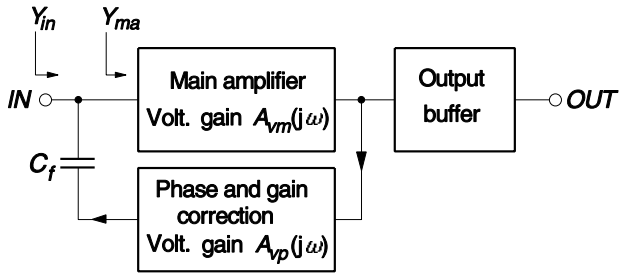

Figure 1: Structure of the feedback amplifier

Input admittance of the amplifier is

$$Y_{in}(j\omega) = Y_{ma}(j\omega) + j\omega C_f\left[1 - A_v \right. \approx Y_{ma} - j\omega C_f \cdot A_{vm}(j\omega) \quad (1)$$

Thus the input matching ($Y_{in} = Y_g$) requires that the correcting network has the response in the form given by

$$A_{vp}(j\omega) \approx -\frac{Y_o - Y_{ma}(j\omega)}{j\omega C_f \cdot A_{vm}(j\omega)} \quad (2)$$

This expression may be approximated fairly accurately in the limited frequency range. The feedback has little effect on the noise parameters of the amplifier [2], provided the feedback capacitance C_f is small.

DESIGN TRADEOFFS

The idea presented may be implemented with careful consideration of several aspects:

- proper selection of C_f and A_{vm};
- stability of the amplifier;
- selection of the input stage transistor geometry.

The tradeoffs in these areas are possible which influence the operating frequency range.

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Extension of the operating range towards low microwave frequencies requires that either C_f be increased or the main amplifier voltage gain is sufficiently high. It may be shown that the increase in C_f results in the deterioration of amplifier noise figure, so the gain of the amplifier should rather be maximized. Because MESFET and HEMT transistors have high output conductance, per-stage voltage gain is low and usually three inverting stages are required.

Amplifier stability may be violated if excess phase shift exists in the amplifier. Detailed and accurate modelling of the amplifier is necessary to predict the response. This circuit was designed with the *Microwave Harmonica* [3] software which contains very accurate models for passive components. Response of portions of the circuit was modelled to 60 GHz to ensure stability. Discrete components design of this amplifier is probably not possible due to large dimensions and additional phase shifts.

One of the problems encountered in the design is the stability of the input stage. The design necessitates the use of wide-gate devices. In such transistors internal feedback loop is formed, as illustrated in Fig. 2. The feedback may cause transistor oscillation, typically in the 20 - 80 GHz range.

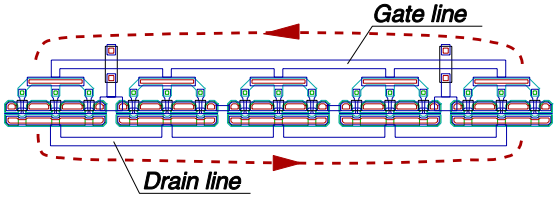

Figure 2: Internal feedback path in the input stage

This loop, which results from the finite reverse isolation (s_{12}), cannot be avoided - only its length may be minimized by proper transistor layout. Loop gain may be minimized by heavy drain line loading, as in the circuit presented, where the cascode input stage was used. Low input impedance of the common gate transistor effectively breaks the loop thus maintaining stage's stability.

INPUT STAGE LOW NOISE DESIGN

The geometry of the input stage transistor results from the requirement of the low noise figure with Z_s = 50Ω, because no on-chip impedance transformation is feasible at low frequencies.

Simplified noise model of the microwave FET [4] valid at low frequencies is presented in Fig. 3

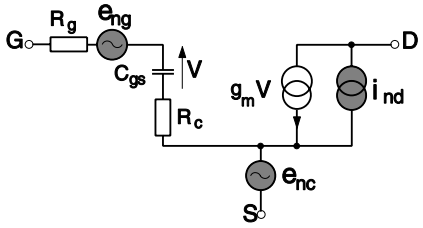

Figure 3: Simplified noise model of the FET

where the noise sources are given by

$$\overline{|^2} = 4kTR_c\,df \qquad \overline{|i_{nd}|^2} = C_n \cdot 2q$$
$$\overline{|^2} = 4kTR_g\,df \qquad (3)$$

T is the transistor channel temperature, R_c is the resistance of the channel portion under the gate ($\approx R_{gs}$), R_g is the gate metallization resistance, and the dimensionless coefficient C_n is the model parameter (typically in the range 0.15 - 0.3).

For the simplified FET model it may be found that the optimum noise source conductance G_{so} is approximately is given by

$$G_{sopt} = \mathrm{Re}\left(\frac{1}{Z_{sopt}}\right) = \omega C_{gs}\left(\frac{K}{1+K}\right. \qquad (4)$$

where K - the coefficient dependent on the drain current, but independent of frequency

$$\overline{4kT_0\,df\,g_m^2 / i_{nd}^2} = g_m\sqrt{2kT_0 / C_n}$$
$$,224 \cdot g_m / \sqrt{C_n I_d} \quad \text{for } T_0 = 290 \qquad (5)$$

Minimum noise figure F_{min} of the transistor is then

$$F_{min} = 1 + \frac{1}{2kT_o\,df} \cdot \frac{(R_g + R_c) \cdot \overline{|}}{} \qquad (6)$$

Thus high G_{so} may be achieved with the wide-gate transistor (high C_{gs}). It may be assumed, that $C_{gs} \div W$ (total gate width), $g_m \div W$, $I_D \div W$ and thus $\overline{|i_{nd}|^2} \div W$, $R_c \div 1/W$ and R_g decreases with W. Increasing transistor width W should not raise the F_{min} significantly, but the increase in C_{gs} limits the upper frequency range of the

broadband low-noise design with input matched. In the amplifier presented the total gate width was 450 µm for 5 transistors connected in parallel. With 3 transistors NF below 1.5 dB is possible in the 1 - 10 GHz range.

CIRCUIT FEATURES

Simplified circuit diagram of the amplifier designed according to considerations presented is shown in Fig. 4. Capacitive feedback aids the input matching in the frequency range of approx. 0.3 - 3 GHz while classical series input inductance and source inductive feedback control circuit response at higher frequencies. Sources of input transistors are grounded and negative gate bias is required (due to limited space no bypass capacitors were possible).

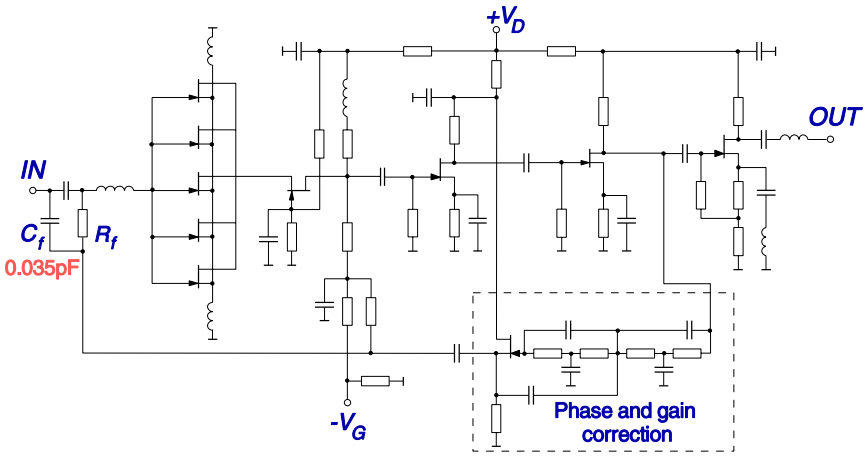

Figure 4: Simplified circuit diagram of the BAMP6 chip

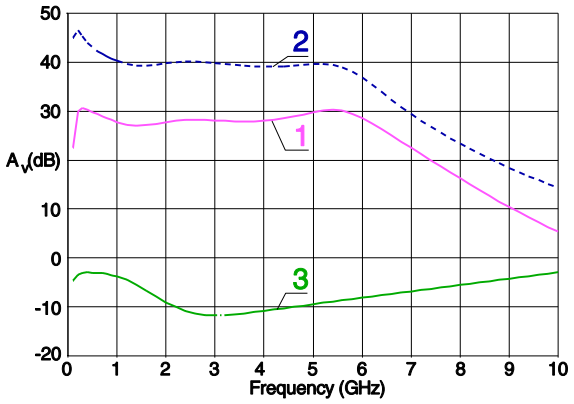

Figure 5: Simulated voltage gain: *1* - entire amplifier, *2* - main amplifier (A_{vm}), *3* - equalizer (A_{vp})

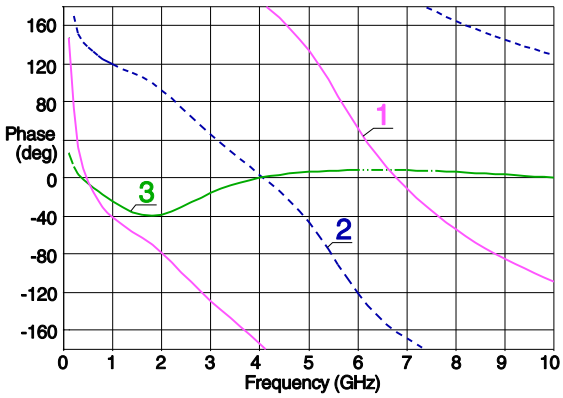

Figure 6: Phase of voltage gain. Labels as in Fig. 2

EXPERIMENTAL RESULTS

The amplifier expected to operate in the frequency range of at least 0.5 - 5 GHz was fabricated in the GaAs technology. The circuit was manufactured in the D02AH 0.2 µm PHEMT process [5] by the *Philips Microwave Limeil* foundry. The layout in shown Fig. 7. Amplifier chips were tested with the *Cascade* on-wafer probing station. Selected results are presented in Figures 8 - 10.

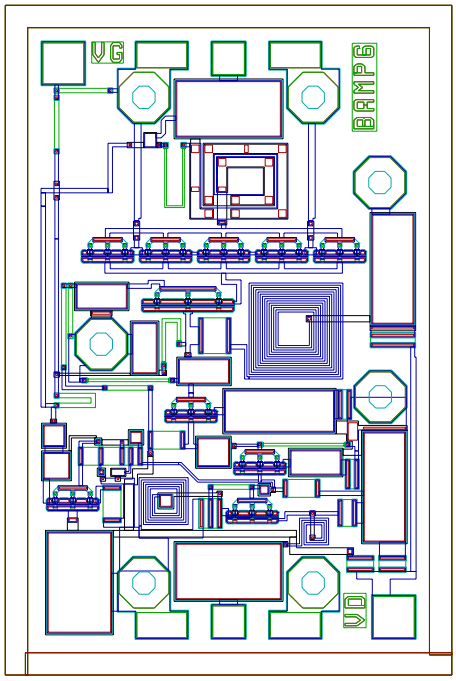

Figure 7: Layout of the amplifier. Chip size is 1 x 1.5 mm

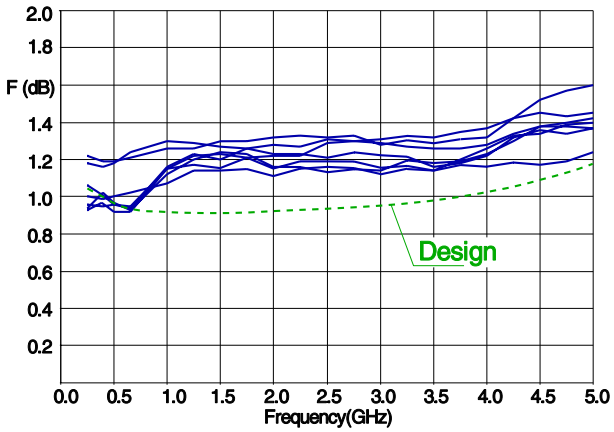

Figure 8: Noise figure versus frequency for several amplifiers

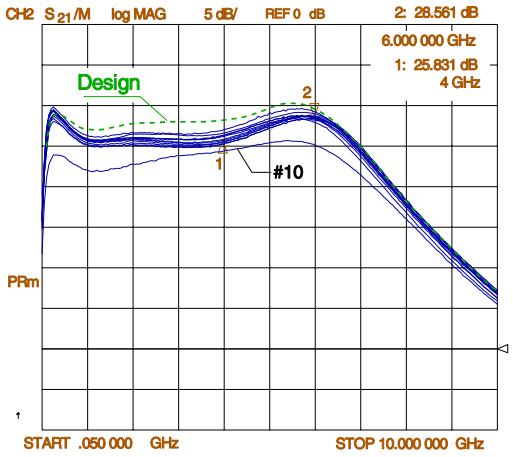

Figure 9: Gain ($|S_{21}|$) and input matching ($|S_{11}|$) for several amplifiers tested at I_D = 50 mA

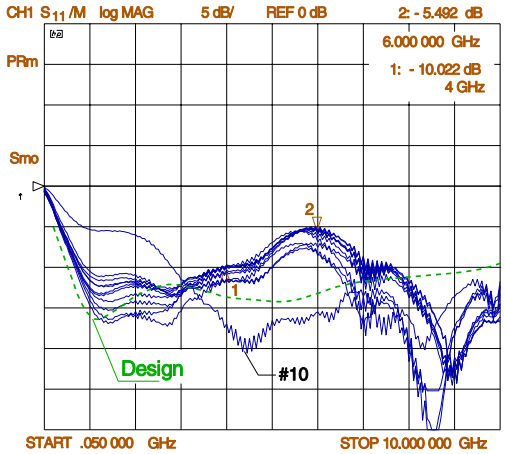

Figure 10: Input matching ($|S_{11}|$) for several amplifiers tested at I_D = 50 mA

Optimally biased amplifier has typical parameters:

- gain 26 dB ±1.5 dB in the 0.25 GHz - 6.5 GHz range,
- noise figure below 1.4 dB to 5 GHz,
- $|S_{11}| \leq$ - 8 dB in the 0.5 - 10 GHz range and ≤-10 dB in the 0.8 - 4 GHz range,
- output reflection is typically better than -12 dB across the 0.8 - 10 GHz range.

Test results indicate that the response of the amplifier is very repeatable due to the *PML* process features. Computer simulation suggests that still better performance is possible with minor adjustments to the prototype. Response at low frequencies is limited by the on-chip input and output coupling capacitors. The circuit is stable under various bias conditions.

CONCLUSIONS

Very low noise broadband MMIC amplifier design concept is presented. The idea of capacitive feedback is feasible with tightly controlled manufacturing process as the Philips' D02AH. Prototype amplifier has response exceeding decade bandwidth with noise figure less than 1.4 dB to 5 GHz and typically less than 1.2 dB to 4 GHz with no components external to the chip.

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